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# Surface Engineering of Reduced Graphene Oxide for Controllable Ambipolar Flash Memories

Su-Ting Han,[†] Ye Zhou,[†] Prashant Sonar,*[,‡] Huaixin Wei,[†] Li Zhou,[†] Yan Yan,[†] Chun-Sing Lee,[†] and V. A. L. Roy*[,†,§]

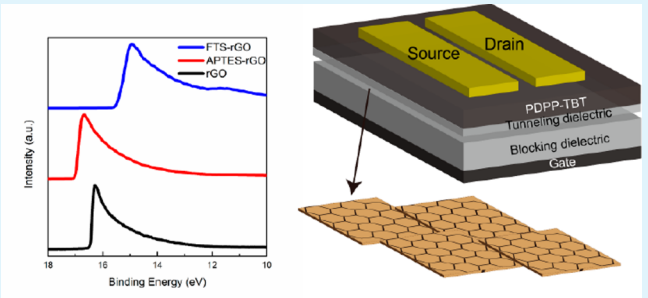
[†]Department of Physics and Materials Science and Center of Super-Diamond and Advanced Films (COSDAF), City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong SAR

[‡]School of Chemistry, Physics and Mechanical Engineering, Queensland University of Technology (QUT), GPO Box 2434, Brisbane, QLD 4001, Australia

[§]Shenzhen Research Institute, City University of Hong Kong, High-Tech Zone, Nanshan District, Shenzhen, 518057, China

Supporting Information

**ABSTRACT:** Tunable charge-trapping behaviors including unipolar charge trapping of one type of charge carrier and ambipolar trapping of both electrons and holes in a complementary manner is highly desirable for low power consumption multibit flash memory design. Here, we adopt a strategy of tuning the Fermi level of reduced graphene oxide (rGO) through self-assembled monolayer (SAM) functionalization and form p-type and n-type doped rGO with a wide range of manipulation on work function. The functionalized rGO can act as charge-trapping layer in ambipolar flash memories, and a dramatic transition of charging behavior from unipolar trapping of electrons to ambipolar trapping and eventually to unipolar trapping of holes was achieved. Adjustable hole/electron injection barriers induce controllable $V_{th}$ shift in the memory transistor after programming operation. Finally, we transfer the ambipolar memory on flexible substrates and study their charge-trapping properties at various bending cycles. The SAM-functionalized rGO can be a promising candidate for next-generation nonvolatile memories.




**KEYWORDS:** *self-assembled monolayer, reduced graphene oxide, work function, flash memory, ambipolar, charge-trapping behavior*

## INTRODUCTION

Charge-trapping behavior including unipolar trapping of either electrons or holes as well as ambipolar trapping of both electrons and holes is one of the most important figures of merit for flash memories.[1−4] In nonvolatile floating gate-based memories, the charge carriers can be stored in the charge-trapping elements after programming operation and erased back to the semiconducting channel by reverse gate bias.[5−9] Threshold voltage ($V_{th}$) can be manipulated since the channel conductance depends on whether the charge carriers are stored in the floating gate or not.[10,11] The charge-trapping types can be justified by the shifting direction of the transfer curve. Employing unipolar charge trapping of either electrons or holes in a complementary manner is highly desirable for low power consumption, while the ambipolar trapping is an efficient approach for designing multilevel data storage memories.[3] In another aspect, ambipolar semiconducting materials have received a lot of interest for mimicking traditional complementary circuits.[12−17] The complexity of the printed logic circuits design could be further reduced by using low band gap ambipolar materials and symmetric electrodes. In addition, investigating the ambipolar material based nonvolatile memories is necessary for the development of ambipolar integrated circuits with unique properties, which may not be achievable with unipolar semiconductors. On this regard, systematic control over the trapping behavior of ambipolar flash memory is critical for various practical applications. It is commonly believed that the charge-trapping behavior of flash memory is governed by the holes or electrons injection from the highest occupied molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO) of semiconductor materials to the Fermi level of charge-trapping elements.[3,18] Tuning the Fermi level of the charge-trapping layer/floating gate in memory transistors can control the hole/electron trapping behaviors. However, because of the fixed Fermi level of metal nanoparticles in the nanofloating gate memory transistor, it is hard to achieve tunable electrical characteristics by manipulating the energy level.[19,20] Therefore, graphene can be a better choice for the charge-trapping layer since its Fermi level can be manipulated.[21,22] Previously, several methods including deposition of conjugated organic molecules,[23] using the Au-ion treatment[21] or ion irradiation,[24] have been introduced to tune the work function of graphene.

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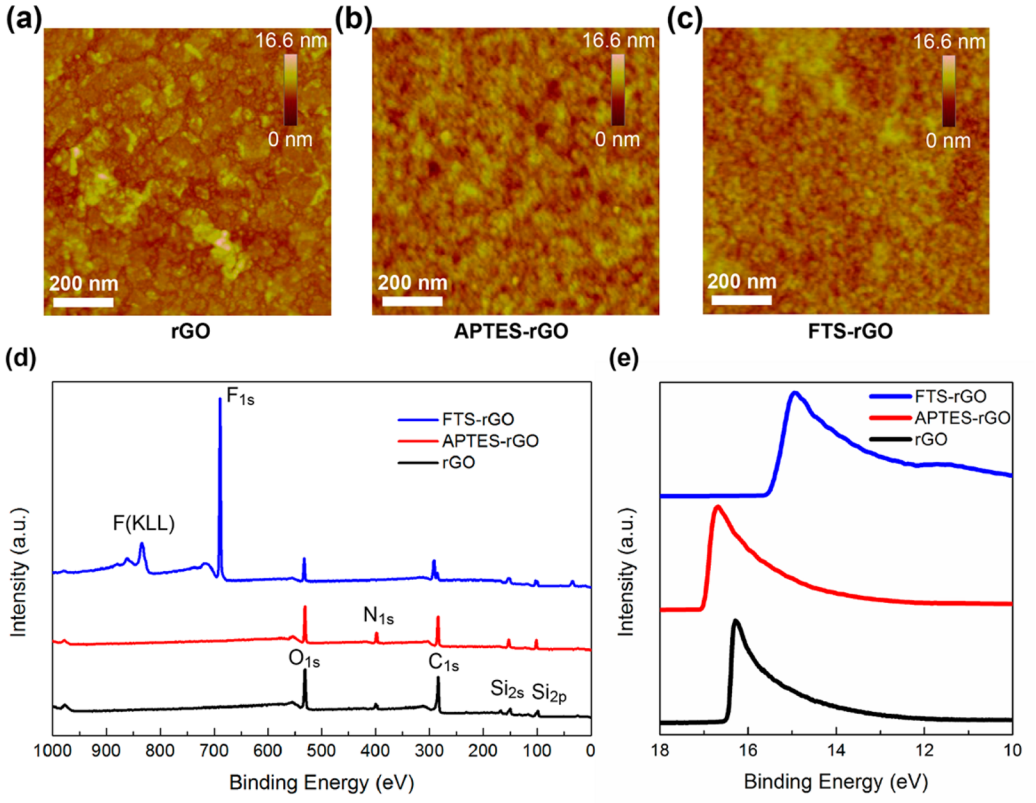


**Figure 1.** Tapping-mode AFM height image of (a) fabricated rGO film, (b) APTES-functionalized rGO, and (c) FTS-functionalized rGO. (d) The XPS data of pristine rGO and SAM-functionalized rGO. (e) UPS spectra of pristine rGO and SAM-functionalized rGO.

Nevertheless, these approaches cannot offer wide-range tuning of the graphene doping level from p-type to n-type. For this reason, alkylsilane with electron-withdrawing or electron-donating groups self-assembled on the graphene is proposed to introduce p-type/n-type doping of graphene with a wide range of manipulation of Fermi level.[25,26] In another aspect, traditional Si-based flash memories usually employ polycrystalline silicon as floating gate or $Si_3N_4$ as charge-trapping layer. The work function of polycrystalline silicon can be tuned by different doping concentration,[27] and the charge-trapping behavior can also be adjusted by tailoring the composition of $Si_3N_4$ layer.[28] However, these materials are always applied on the rigid substrate, which is not compatible with flexible electronics. Reduced graphene oxide (rGO) and its derivatives can be synthesized through a cheap solution-processed method, which is also highly transparent. These advantages make rGO more suitable to apply in the flexible flash memory with tunable charge-trapping behavior. Recently, some works reported on graphene and its derivatives-based flash memories;[29] however, few of them utilized rGO with tunable work functions to manipulate the charge-trapping behavior of the flash memories.

Herein, we present a simple approach to systematically modulate the trapping behavior of polymer ambipolar flash memory by utilizing alkylsilane self-assembled monolayer (SAM) functionalized rGO as charge-trapping layer. The ambipolar polymer material, poly(diketopyrrolopyrrolethiophenebenzothiadiazolethiophene) (PDPP-TBT) is employed as active layer. Two kinds of alkylsilane compounds, namely, (tridecafluoro-1,1,2,2,-tetrahydrooctyl) trichlorosilane (FTS) with electron-withdrawing group and aminopropyl triethoxysilane (APTES) with electron-donating group are selected to introduce p-type and n-type doping of the rGO layer, respectively. The systematic shifts of the Fermi level of rGO induces a dramatic transition of the charging behavior from unipolar trapping of electrons to ambipolar trapping and eventually to unipolar trapping of holes. The doping process of rGO was investigated by X-ray photoemission spectroscopy (XPS). Ultraviolet photoemission spectroscopy (UPS) was used to characterize the work function of rGO after SAM doping. The narrowed holes/electrons injection barrier originated from the Fermi level shifts of functionalized rGO layer have strong contribution to the ambipolar/unipolar charging behavior alteration when considering the HOMO/LUMO level of PDPP-TBT. Our device fabrication techniques, including synthesis of rGO sheets, formation of rGO layers, and alkylsilane self-assembled onto the rGO layers, are all based on low-temperature solution-processed method, and we have also demonstrated the ambipolar memory transistor on flexible substrates to achieve low-voltage operation.

## RESULTS AND DISCUSSION

The fabricated rGO film contains a few layers of rGO sheets. The precleaned $SiO_2/Si$ substrate is fully covered by rGO sheets through simply spin-casting the rGO solution with an average rGO sheet size of 200 nm. Utilization of alkylsilane molecules to form SAM functionalization on the rGO film was obtained through dipping process, while the SAM reagents were coupled to the rGO surface directly. The atomic force microscopy (AFM) images indicating the effect of APTES and FTS SAMs on the morphology of rGO layer are illustarted in Figure 1a–c. The thickness of rGO film is ~5 nm. The small bumps nucleated due to SAM functionalization can be observed. The X-ray photoelectron spectroscopy (XPS) was utilized to investigate the growth of SAMs on rGO surface. As shown in Figure 1d, the XPS


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spectrum of pristine rGO exhibits four peaks at 530, 284, 157, and 106 eV, which correspond to $O_{1s}$, $C_{1s}$, $Si_{2s}$, $Si_{2p}$, respectively.[30] The existence of numerous oxygen-containing functional groups on rGO plays a significant role for the covalent bonding of FTS and APTES with rGO.[31] APTES molecules can graft onto the rGO surface (APTES-rGO) by its amino group reacting with the epoxy group of rGO.[32] It is reasonable that the $N_{1s}$ signal at 400 eV is relatively small since there are fewer epoxy groups than hydroxyl groups on rGO.[26] However, the hydroxyl groups can act as nucleation sites to prompt the assembly of FTS on rGO.[33] The peaks observed at 862, 835, and 689 eV correspond to F (KLL) and $F_{1s}$ in the XPS spectrum of FTS-functionalized rGO (FTS-rGO). The nitrogen and fluorine signal of APTES-rGO and FTS-rGO demonstrate successful covalent doping of rGO films with APTES and FTS. XPS C 1s spectra of pristine rGO, APTES-rGO, and FTS-rGO are shown in Supporting Information (Figure S1). C−N signal can be observed in APTES-rGO, indicating that the amino moieties react with the epoxy groups on rGO surface. C−$CF_2$ and O−$CF_2$ signal can be found in the FTS-rGO, demonstrating the successful functionaliztion.[34] The energy spectra of SAMs functionalization of rGO were further investigated by ultraviolet photoelectron spectroscopy (UPS) as depicted in Figure 1e. A gold plate was used for the calibration in the experiment. The vacuum level of the tested samples was determined by linear extrapolation of secondary electron cutoffs on the high-binding energy side of the UPS spectra (14−18 eV).[35] The work function (WF) was calculated by subtracting $E_{SE}$ from $h\nu$, where $E_{SE}$ and $h\nu$ are the secondary edge position and the incident photon energy (21.2 eV).[36] The WF of rGO is calculated to be ~4.74 eV, which is consistent with the reported value of chemically rGO.[37,38] Compared with the pristine rGO, the APTES-rGO sample displays n-doped property with the decreased WF of 4.21 eV, while the FTS-rGO sample is intensely p-doped with the increased WF of 5.70 eV. The WFs of the SAM-functionalized rGO samples vary more widely compared with Au ion-doped rGOs (increase the WF from 4.4 to 5.0 eV[39]), suggesting that direct surface engineering of rGO can induce efficient doping. Previous reports show that the carrier concentration of rGO varies with the SAM functionalization and that the doping of rGO leads to the tunable work function.[26] The upward shift of Fermi level of APTES-rGO is mainly attributed to the electron-donating group of APTES molecules, electrostatic potential created by the dipole moment of APTES, while the electron-withdrawing characteristics of FTS and protonic doping via unreacted silanol groups induce the increased WF of FTS-rGO.[39−41]

Figure 2a shows an illustration of the three-dimensional (3D) structure for bottom-gate top-contact ambipolar flash memory devices and the chemical structure of the ambipolar materials PDPP-TBT and alkysilanes (APTES and FTS). Silicon wafers with 300 nm thick $SiO_2$ layers serve as the gate electrodes and blocking dielectric layers. After spin-coating the rGO films, the substrates were then immersed into the APTES and FTS solutions to form the monolayers. Then another 5 nm atomic layer deposited (ALD) aluminum oxide ($Al_2O_3$) was deposited as tunneling dielectric layer to prevent charge leakage from the doped rGO layer to the semiconductor layer as well as to decrease the electrostatic force from SAMs layers, which may affect the charge transport in semiconductor layer. It is worth noting that the $Al_2O_3$ deposition was performed at 80 °C. The thermal stability of work function value can be well-maintained at the temperature lower than 800 °C.[42] In another aspect, the FTS

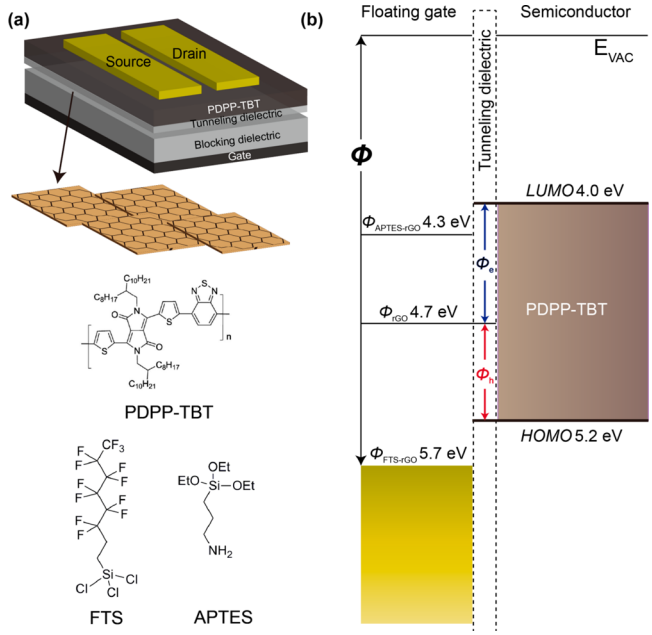


**Figure 2.** (a) Three-dimensional schematic illustration of the ambipolar memory device, chemical structure of PDPP-TBT, and the used alkysilane in the experiment: aminopropyl triethoxysilane (APTES) and (tridecafluoro-1,1,2,2,-tetrahydrooctyl) trichlorosilane (FTS). (b) Energy band diagrams of SAM-doped rGO and the semiconducting polymer PDPP-TBT.

and APTES are covalently bonded to rGO, which is also stable at 80 °C. The scanning electron microscope (SEM) images of the APTES-rGO and FTS-rGO films are shown in Supporting Information (Figures S2 and S3). Finally, the ambipolar PDPP-TBT was spin-coated as an active layer followed by the thermal evaporation of 40 nm of Au as source/drain electrodes. The synthesis procedure of PDPP-TBT can be found in the literature.[13] Figure 2b represents the schematic diagram of energy levels of the SAM-doped rGO and ambipolar polymer in the memory transistors, where the $\Phi_e$ and $\Phi_h$ are barrier heights of carrier injection at the interface for electrons and holes, respectively.

Figure 3a,b shows the typical output characteristics of the fabricated ambipolar field-effect transistors (FET) at hole-enhancement type and electron-enhancement type, respectively. The devices without embedding the rGO sheets (device structure: Si/300 nm $SiO_2$/5 nm $Al_2O_3$/PDPP-TBT/Au source-drain) were fabricated as control devices to determine the charging effects in the transistor structure. Unless otherwise mentioned, all the device structures and the processing conditions are the same compared with the ambipolar memory devices except the insertion of rGO layers. The transistors are operated in both hole-enhancement mode and electron-enhancement mode. The drain-source current $I_{DS}$ increases exponentially with increasing drain-source voltages ($V_{DS}$) at relative low gate-source voltages ($V_{GS}$). Figure 3c,d shows the transfer curves of initial states and different programmed states (±90 V) in p-type operation and n-type operation, respectively. Hole-enhancement mode can be observed at $V_{GS} < -26.3$ V with $V_{DS}$ of −50 V, while electron-enhancement mode is obtained at $V_{GS} > 20.6$ V at $V_{DS} = 50$ V. The electron and hole mobilities at the saturation regime are $1 \times 10^{-2}$ $cm^2$ $V^{-1}$ $s^{-1}$ and $2 \times 10^{-4}$ $cm^2$ $V^{-1}$ $s^{-1}$, respectively. A negligible memory window was observed after applying bias pulses of ±90 V for 1 s in either hole-


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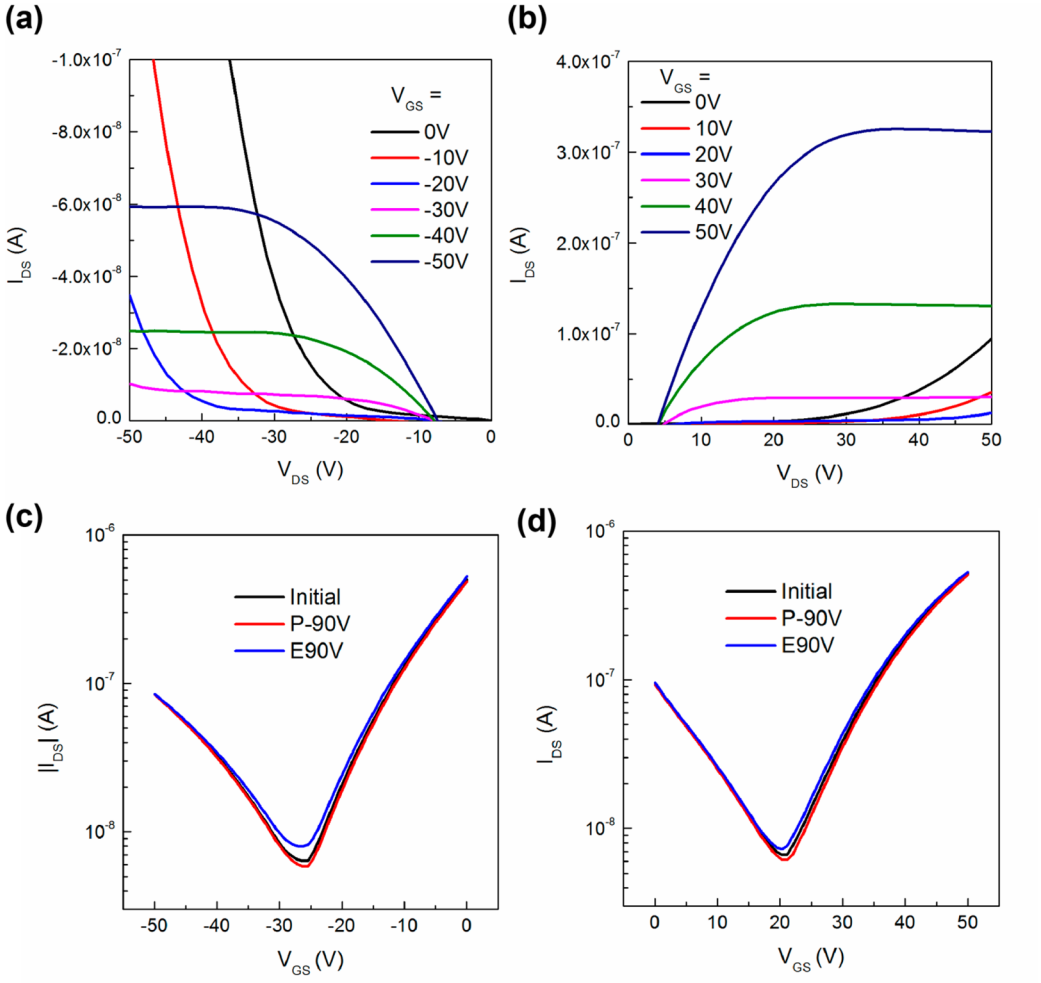


**Figure 3.** Initial output characteristics of the ambipolar transistor at (a) hole-enhancement mode and (b) electron-enhancement mode. Transfer curves of the ambipolar transistor before and after programming at ±90 V for 1 s at (c) p-type enhancement mode and (d) n-type enhancement mode.

enhancement or electron-enhancement mode, implying almost no charging/discharging effect occurred for the charge carriers in the bulk or at the interfaces of the gate dielectric layer.

Subsequently, the charge-trapping behavior of ambipolar memory devices was studied. The transfer characteristics of the memory devices based on rGO (denoted as rGO device), APTES-rGO (denoted as APTES-rGO device), and FTS-rGO (denoted as FTS-rGO device) after different programming operations (±90 V for 1 s) at the p-type enhancement mode and n-type enhancement mode are shown in Figure 4. Almost no decrease in the charge mobility of the ambipolar polymer was observed after embedding pristine rGO and SAM-doped rGO in $Al_2O_3$ layer, which is satisfactory enough to ensure efficient operation. The $V_{th}$ value varied in the initial state after inserting the pristine rGO and SAM-functionalized rGO compared with standard FET device. The $V_{th}$ shifts are originated from presence of traps and relatively rough interface introduced by rGO charge-trapping layers. The $V_{th}$ of initial state (denote as $V_{th}$ (initial)), $V_{th}$ of negative programmed state (denoted as $V_{th}$ (negative programmed)), and $V_{th}$ of positive programmed state (denoted as $V_{th}$ (positive programmed)) of all the devices are summarized in Table 1. For rGO device, after the application of negative bias in gate electrode, $V_{th}$ is shifted toward the negative direction, and after applying positive bias, $V_{th}$ is shifted toward the positive direction at both p-type enhancement mode and n-type enhancement mode. The negatively shifted $V_{th}$ shows that more and more holes are trapped in the process, and the potential evolved from these traps screens the gate voltage after applying −90 V at the gate, while the stored holes are compensated by electrons; electrons are eventually trapped in the rGO layer due to the additional positive bias of +90 V. It can be seen that both electrons and holes participate in the charge-trapping process in the rGO device during the programming operation.[3] Well-balanced $V_{th}$ shifts obtained after negative and positive programming operations reveal ambipolar trapping capability of rGO device. In contrast to ambipolar trapping observed in rGO device, hole-trapping of APTES-rGO device could not be evaluated because $V_{th}$ shift was negligible after applying negative bias in gate electrode, while electron-trapping of FTS-rGO device was difficult to achieve since $V_{th}$ shift was insignificant after positive programming operation. More than 10 devices have been measured, and similar electrical characteristics can be observed. Direct tunneling (at relatively low voltage) and Fowler−Nordheim (F−N) tunneling (at relatively high voltage) are considered as the favorable routes in program/erase operations rather than the channel hot hole/electron injection due to the low drift velocity of charge carriers in ambipolar polymer.[43,44] In the programming operation, the electrical field across the tunneling dielectric layer could be calculated by the following equation[4]


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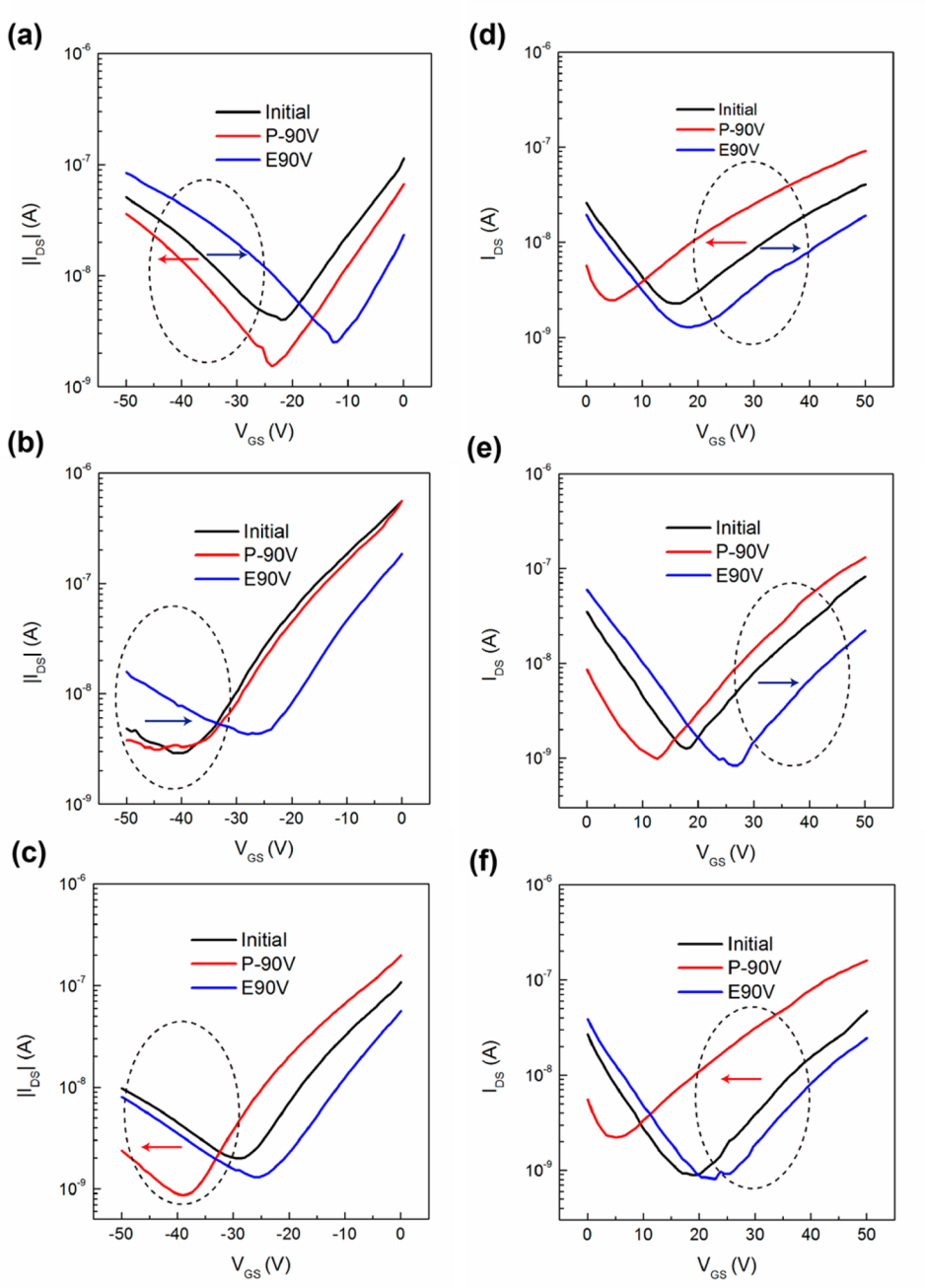


**Figure 4.** Electrical characteristics of ambipolar memory transistors based on (a) undoped rGO, (b) APTES-functionalized rGO, and (c) FTS-functionalized rGO at hole-enhancement mode. Electrical characteristics of ambipolar memory transistors based on (d) undoped rGO, (e) APTES-functionalized rGO, and (f) FTS-functionalized rGO at electron-enhancement mode.

**Table 1. Measured $V_{th}$ of initial states, programmed states at different operation modes**

| | hole-enhancement mode | | | electron-enhancement mode | | |
|---|---|---|---|---|---|---|
| | $V_{th}$ (initial) [V] | $V_{th}$ (negative programmed) [V] | $V_{th}$ (positive programmed) [V] | $V_{th}$ (initial) [V] | $V_{th}$ (negative programmed) [V] | $V_{th}$ (positive programmed) [V] |
| rGO | −18 | −25 | −12 | 15 | 5 | 26 |
| APTES-rGO | −15 | −16 | 0.5 | 25.5 | 23.5 | 37 |
| FTS-rGO | −20 | −35 | −19 | 24 | 7 | 27 |
| flexible APTES-rGO | −3 | −3.4 | −1.4 | 1.4 | 1.3 | 3.2 |

$$E_1 = \frac{V_{GS}}{d_1 + d_2(\varepsilon_1/\varepsilon_2)} + \frac{Q}{\varepsilon_1 + \varepsilon_2(d_1/d_2)} \quad (1)$$

where $\varepsilon_i$ are the dielectric constants, $d_i$ is the thickness of the two dielectric layers, and $Q$ is the stored charge carrier on the rGO layers. At the initial stage of the ambipolar memory device



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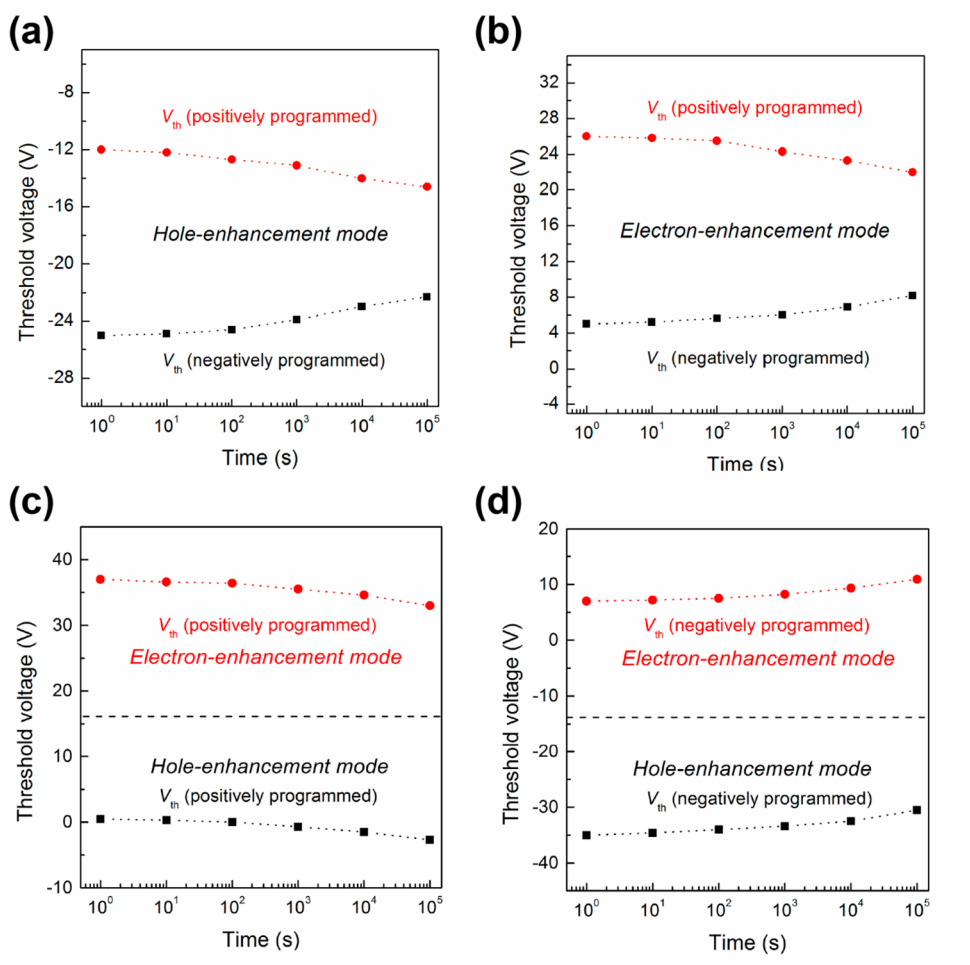


**Figure 5.** Retention properties of (a, b) rGO device, (c) APTES-rGO device, and (d) FTS-rGO device at different operation modes.

operation ($Q$ = 0 and $V_{GS}$ = ± 90 V), the electrical field in the $Al_2O_3$ tunneling dielectric layers for these three devices is estimated to be 1.78 MV/cm$^2$. In general, high electrical field in the tunneling dielectric layer would promote an efficient injection of both holes and electrons from the ambipolar semiconductor to the charge-trapping layer and trapping in charge-trapping layer, however, which is inconsistent with unbalanced charge trapping observed in the APTES-rGO device and FTS-rGO device. These results show that the charge-trapping behavior varies with the SAM functionalization. In the rGO-based memory transistors, the charge carriers can be stored in the Fermi level of rGO domains surrounded by the band gap of tunneling and blocking dielectrics. Considering similar applied electrical fields of these three devices, the distinctive charge-trapping behaviors are mainly attributed to the difference of energy levels since the programming operation is inversely proportional to the injection barrier arising from the Fermi level of the floating gate and HOMO/LUMO levels of semiconductor layer.[3,18] Fermi level of pristine rGO is centered between the HOMO level and LUMO level of PDPP-TBT with the hole injection barrier of 0.5 eV and electron injection barrier of 0.7 eV, suggesting a comparable tunneling rate of holes and electrons. The easier positive programming process and harder negative programming process of APTES-rGO device can be explained by the narrowed electron injection barrier of 0.3 eV and extended hole injection barrier of 0.9 eV, which are induced by up-shifting Fermi level of APTES-rGO. Similarly, the reason for the unipolar trapping of holes observed in FTS-rGO device is due to the huge electron injection barrier height of 1.7 eV, which originates from the strong p-doping of FTS-rGO. The cumulative $V_{th}$ shifts as a function of bias time are shown in Supporting Information (Figure S4). $V_{th}$ shift increases with the increased programming/erasing operation time. The plot of the memory windows versus various gate voltages is shown in Supporting Information (Figure S5). We increased the programming/erasing ($P/E$) voltages from ±70 V to ±90 V for the ambipolar memory devices. In general, enhancing the $P/E$ voltage will increase the probability of tunneling events and therefore increase the number of trapped/detrapped charge carriers.

It is imperative that the retention time should be sufficient for long-term stable data storage. Figure 5 shows retention characteristics of rGO device, APTES-rGO device, and FTS-rGO device in the hole-enhancement and electron-enhancement mode, respectively. The stored data has an estimated retention time of as high as ~$10^5$ s, which is comparable to other types of flash memory devices. Vertical loss of the stored charges may usually originate from the charge-carrier diffusion from the rGO sheets through the tunneling $Al_2O_3$ layer. In our designed system, the rGO/$Al_2O_3$ structure offers a large barrier height to maintain the trapped holes/electrons in rGO. The retention property of the ambipolar memory at high temperature (80 °C) is also investigated and shown in the Supporting Information (Figure S6). The data retention ability is sensitive to the temperature, and it reduces with increased temperature due to thermal excitation


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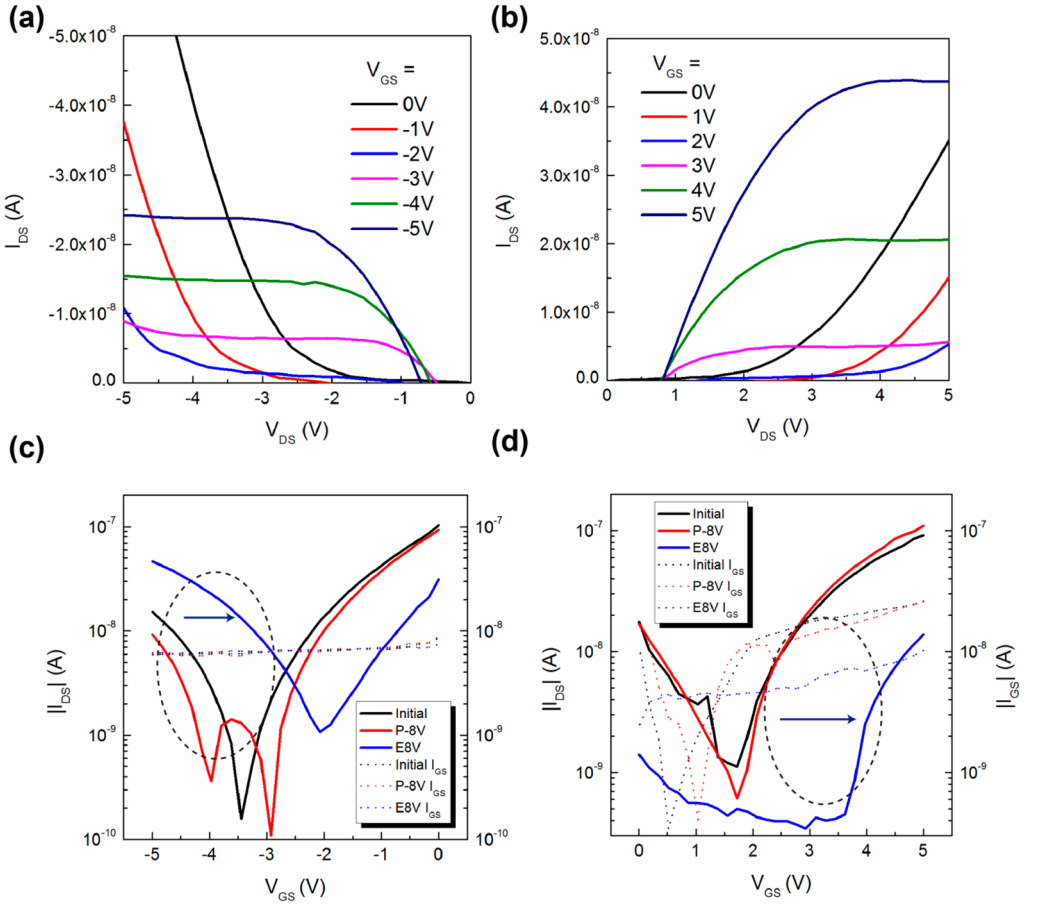


**Figure 6.** Output characteristics of the flexible memory device based on APTES-rGO at (a) hole-enhancement mode and (b) electron-enhancement mode. Transfer curves of the flexible memory device before and after programming the gate (±8 V for 1 s) at (c) hole-enhancement mode and (d) electron-enhancement mode.

of trapped charge carriers.[45] The large available thermal energy at higher temperature induces inferior quantum confinement effects and increases the possibility of charge loss over time.

The tunable charge-trapping properties of the ambipolar memory based on SAM-functionalized rGO has been further extended to flexible substrates toward the realization of next-generation soft electronics. We fabricated flexible memory transistors based on APTES-rGO with low-voltage operation. A 25 nm thick silver (Ag) gate electrode was deposited on the (polyethylene terephthalate) substrate as gate electrode. A 15 nm thick aluminum oxide $Al_2O_3$ (blocking dielectric layer) and 5 nm thick $Al_2O_3$ (tunneling dielectric layer) were atomic layer deposited, and the APTES-rGO charge-trapping layer was inserted between them. The typical output curves of the flexible ambipolar memory devices based on APTES-rGO under low-voltage operations are shown in Figure 6a,b. The saturation of the $I_{DS}$ is observed at both high positive and negative $V_{GS}$ values, indicating electrons and holes are accumulated at the respective $V_{GS}$. At low $V_{GS}$, the transistors show diode-like curves with a rapid increase of $I_{DS}$ with $V_{DS}$, which can be attributed to the presence of both charge carriers in the channel. The memory characteristics were further examined by measuring the $V_{th}$ shift with respect to different programming operations (±8 V for 1 s). Figure 6c,d displays the transfer curves in hole-enhancement and electron-enhancement mode, respectively. The $V_{th}$ (initial), $V_{th}$ (negative programmed), and $V_{th}$ (positive programmed) of flexible APTES-rGO device are −3, −3.4, and −1.4 V in p-type operation and 1.4, 1.3, and 3.2 V in n-type operation. A negligible memory window after the negative programming opeartion and large $V_{th}$ shift after the positive programmed operation imply uniploar trapping of electrons, which is in good agreement with the performance of high-voltage operated APTES-rGO device on the rigid substrate. The relatively large gate current can be eliminated by the further modification of tunneling dielectric layer.

Figure 7a displays retention characteristics for flexible APTES-rGO device. The $V_{th}$ (positively programmed) values at both hole-enhancement and electron-enhancement modes could be maintained for more than $10^5$ s. Furthermore, we examined the $V_{th}$ of negatively programmed and positively programmed states under a bending radius of curvature of 1 cm (tensile and compressive strain of ±1%) as shown in Figure 7b. The flexible memory transistors based on APTES-rGO at both hole-enhancement and electron-enhancement modes did not exhibit obvious degradation of $V_{th}$ after 500 bending cycles as demonstarted in Figure 7c,d. During the bending test, our flexible memory transistors exhibit excellent mechanical properties, demonstrating the potential application in flexible integrated circuits. Another important reliability test for nonvolatile memory devices is endurance performance.[29,46,47] The endurance properties of the flexible ambipolar memory device are shown in Supporting Information, Figure S7. These data states of the memory devices were well-maintained, and the whole data level range did not degrade for over 500 $P/E$ cycles.



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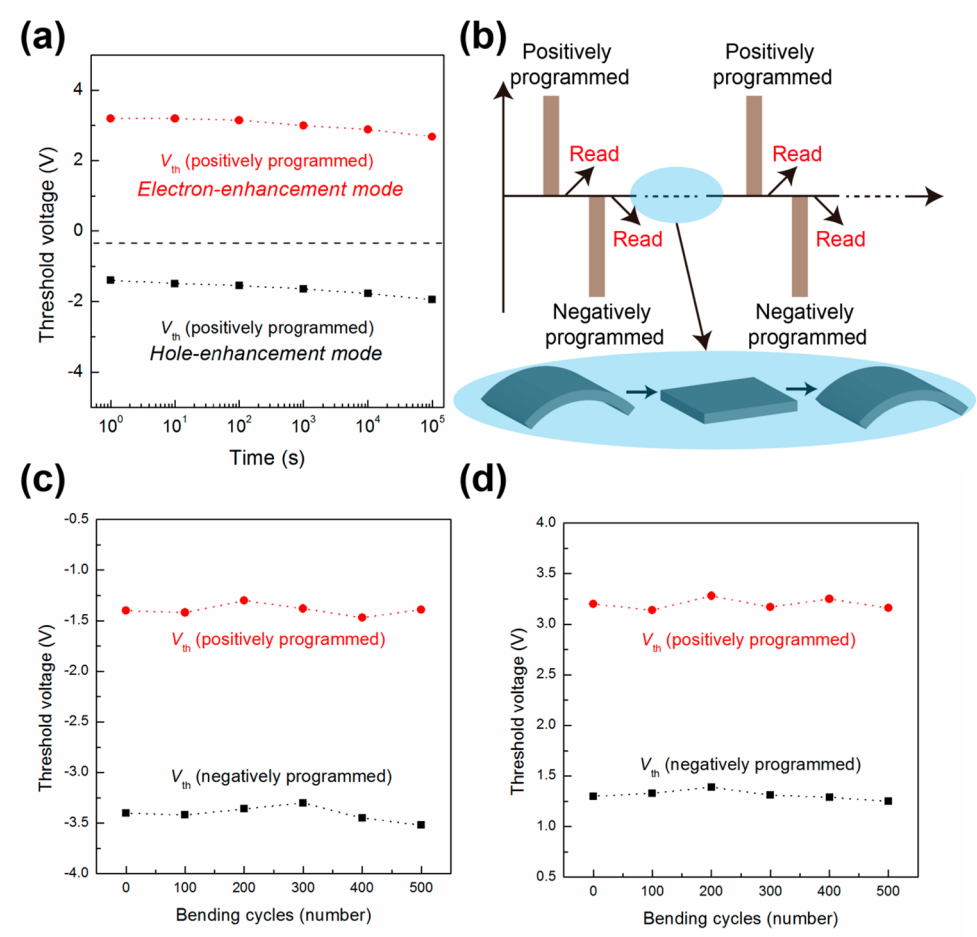


**Figure 7.** (a) Retention properties of flexible ambipolar flash memory based on APTES-rGO. (b) Illustration of the bending tests. Mechanical stability tests of flexible ambipolar flash memory at (c) hole-enhancement mode and (d) electron-enhancement mode.

## CONCLUSION

In summary, the SAM-doped rGO is first utilized as charge-trapping element in ambipolar flash memory. Upward and downward shifting of the Fermi level of rGO were achieved via direct surface functionalization using APTES and FTS SAMs, respectively. The UPS results evidence that the work functions vary in a wide range from 4.3 to 5.7 eV, which is superior to the conventional chemically doped rGO. After inserting the doped and undoped rGO between the blocking and tunneling dielectric layers, a transition from ambipolar trapping of both holes and electrons in rGO device to unipolar trapping of electrons/holes in APTES-rGO/FTS-rGO devices occurred. The energy level alignment plays a critical role in the device performance. The adjustable hole/electron injection barriers induce the significant $V_{th}$ shift after positive/negative programming operation and negligible $V_{th}$ shift after application of negative/positive gate bias. The unipolar electron-trapping properties of flash memory based on APTES-rGO were further demonstrated on the flexible substrate. It is believed that SAM-doped rGO-based ambipolar memory cells can bring the development of polymer nonvolatile memory device a step closer to functional applications in next-generation flexible electronics.

## METHODS

**Preparation of rGO and SAM Functionalization.** Graphite oxide was synthesized using Hummer's method. Graphite oxide (12.5 mg) was then suspended in 25 mL of deionized water to form brown dispersion. Ultrasonication was taken for 1 d to exfoliate the graphite oxide into graphene oxide (GO). Hydrazine monohydrate (10 $\mu$L) was added to the homogeneous yellow-brown 10 mg mL$^{-1}$ GO solution in a mixture of *N*,*N*-dimethylformamide (DMF) and water in a volume ratio of 9:1, and the solution was heated with vigorous stirring at 80 °C for 12 h. A small amount of poly(vinyl alcohol) (weight ratio of GO/PVA is 10:1) was used as an additive to prevent the agglomeration of the well-dispersed rGO solution. A homogeneous colloidal suspension of RGO was spin-cast onto Si wafers. The substrates were then transferred to SAM reactors. FTS was reacted with the surface of the rGO film in anhydrous *n*-hexane solvent for 2 min, and APTES was reacted in anhydrous toluene solvent (20 mL) for 90 min to compensate for its low reactivity. The concentration of FTS and APTES in the organic solution is 25 $\mu$L/10 mL.

**Device Fabrication.** Ambipolar memory transistors were fabricated on heavily n-doped Si wafers with 300 nm of $SiO_2$ as gate dielectric layer. Low-voltage flexible memory transistors were fabricated on 200 $\mu$m thick PET substrate with 15 nm of $Al_2O_3$. The PDPP-TBT films were formed on the substrates by spin-coating from 7 mg mL$^{-1}$ PDPP-TBT in chloroform solution, and thermal annealing at 160 °C for 30 min was then carried out in nitrogen glovebox. The $Al_2O_3$ tunneling and blocking layers were deposited using a Savannah 100 ALD system, while the substrate temperature was kept at 80 °C. Patterned 40 nm gold electrodes with a channel length of 50 $\mu$m and width of 1000 $\mu$m were thermally evaporated through a shadow mask under $3 \times 10^{-6}$ Torr base pressure.

**Characterization.** The thicknesses of layers ($SiO_2$, $Al_2O_3$, and PDPP-TBT) were checked with the ellipsometer. The morphologies of


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SAM-functionalized rGO were examined by AFM (Veeco Multimode V). The photoemission measurements were performed in a VGESCALAB 220i-XL UHV surface analysis system with a base vacuum of $1 \times 10^{-10}$ Torr. The tested samples were prepared on the precleaned silicon substrate and then transferred into the chamber. A monochromatic Al K$\alpha$ X-ray source (1486.6 eV) was adopted to investigate the possible interfacial chemical reactions and changes of energy level when doing the XPS measurement. A He discharge lamp (21.2 eV) with 90 meV instrumental energy resolution as valued from the Fermi edge of a cleaned Au plate was used to measure the valence structure of the sample when doing the UPS measurement. All the samples were biased at −5 V with respect to ground for efficient collection of the secondary electrons. The electrical performances of the memory devices were characterized by a Keithley 2612 source meter in nitrogen glovebox at room temperature.

## ■ ASSOCIATED CONTENT

### Supporting Information

C 1s XPS spectra and SEM images of the SAM-rGO, memory window with respect to various P/E time and voltage, retention property of the flexible device at 80 °C, and the P/E endurance characteristics of the flexible device. This material is available free of charge via the Internet at http://pubs.acs.org.

## ■ AUTHOR INFORMATION


### Corresponding Authors

*E-mail: val.roy@cityu.edu.hk. (V.A.L.R.)
*E-mail: sonar.prashant@qut.edu.au. (P.S.)


### Notes

The authors declare no competing financial interest.

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